This survey collects your answers for the PIKA on Kirk & Hwu chapter 5 in CPSC 418 2017-2. In order to receive PIKA credit, you must enter your name and student number below.

Enter your last name (as it appears in Connect).

Enter your student number.

For each of the questions below, select the best answer. Note that some answers may not be correct for any question, and some questions may have multiple correct answers (although you only need to select one answer for each question). Note that answers which are nouns may refer to the singular or plural case; for example, the answer "lane" should be chosen if the best answer is "lane" or "lanes".

	bank	bypass	channel	coalescing	divergence	lane
Allows load operations from multiple threads to be treated as a single memory access.	○	○	○	○	○	○
Contains multiple banks.	○	○	○	○	○	○
Potential outcome of branching statements in a kernel.	○	○	○	○	○	○
Allows CPUs and GPUs to fully utilize off-chip memory bandwidth even though it takes much more time to get the data out of the DRAM cells in the memory chip than to transfer it across the bus.	○	○	○	○	○	○
Allows CPUs and GPUs to achieve off-chip memory bandwidth much higher than that supported by a DDR / GDDR memory bus.	○	○	○	○	○	○

If a single precision floating point array of size 1024 rows by 1280 columns is stored in row-major order in memory, how far apart are the addresses (in bytes) of two elements which are in the same row but separated by 32 columns? Remember that single precision floating point values require 4 bytes each of memory.

If a single precision floating point array of size 1024 rows by 1280 columns is stored in row-major order in memory, how far apart are the addresses (in bytes) of two elements which are in the same column but separated by 32 rows? Remember that single precision floating point values require 4 bytes each of memory.

If our memory bus can transfer data 10 times faster than we can access it from a single memory chip, what is the minimum number of banks needed to fully utilize the bus?

Consider the "improved reduction kernel" in Kirk & Hwu figure 5.15. If we start with a blockDim of 1024, how many warps will show divergence during the 2nd iteration of the loop?

For the reduction problem in the previous question, how many warps will show divergence during the 7th iteration of the loop?

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