CpSc-418 **Midterm** Oct. 23, 2001

HINT: Brief answers are good. Show your work for calculations. Sentence form answers should be short and to the point.

1. (5 points) What is your name?

2. (35 points) **AFRAID**
   This question is specifically about the paper: *AFRAID – A Frequently Redundant Array of Independent Disks.*
   (a) (5 points) What problem does the paper address?
   (A one or two sentence answer is best).
   (b) (10 points) What are three key observations that lead to the solution presented in the paper?
   (One sentence per observation).
   (c) (5 points) What is the solution presented in the paper?
   (Your answer should have one to three sentences)
   (d) (5 points) What is "parity lag"? Explain what it has to do with AFRAID. (Your answer should have three or four sentences)
   (e) (10 points) What is Amdahl's Law? Amdahl's Law is usually used to describe performance. State an equivalent law about reliability. What does this have to do with the AFRAID paper? (Your answer should consist of two or three sentences and the deriviation of a formula.)

3. (20 points) **Moore's Law**
   (a) (5 points) What is Moore's Law?
   Give the original statement and the current version.
   Give a one sentence explanation of what it means.
   (b) (5 points) What implications does Moore's Law have for hardware design?
   (Your answer should have one or two sentences.)
   (c) (5 points) What implications does Moore's Law have for software design? (Your answer should have one or two sentences.)
   (d) (5 points) How long has Moore's Law been valid?
   State two limitations that may affect Moore's law in the future. (You can just name them or write one or two sentences.)

4. (25 points) **Caching**
Consider the following program fragment (we won't consider *why* anyone would write such an inefficient piece of code):

```
double a[2500];
double sum = 0.0;
for(int i = 0; i < 1000; i++)
    for(int j = 0; j < 2500; j++)
        sum += a[j];
```

Assume that this fragment runs on a machine with a 16Kbyte, direct mapped, L1 data cache, with 64 byte cache lines and a LRU replacement policy. Assume a 10 ns. miss penalty. A double is eight bytes. Assume sum is held in a register. Assume that the L1 cache is empty at when the fragment starts executing.

(a) (10 points) How many data cache misses occur while executing this code?
Classify these misses.

(b) (5 points) What is the total miss penalty when executing this fragment?

(c) (5 points) Now, add a 16 entry victim cache.
The L1 miss penalty is 2ns when the data is available in the victim cache.
What is the total miss penalty with a victim cache?

(d) (5 points) Now, add four stream prefetch buffers (and no victim cache).
The L1 miss penalty is 2ns when the data is available in a stream prefetch buffer. Assume that the prefetch buffers are not limited by prefetch bandwidth.
What is the total miss penalty with a stream prefetch buffers?

5. (20 points) **Terms of the Midterm**
Define each term below. Write one or two sentences per definition **and** cite a paper from the reading list where the term was defined (the title, or the first few words of the title are an adequate citation).

(a) (5 points) Slip sparing

(b) (5 points) TPC-C.

(c) (5 points) Virtual output queueing.

(d) (5 points) Write once