CpSc-418 | Midterm Exam | March 6, 1997

Maximum Marks: 100 | | Time: 80 minutes

Midterm Exam

1. *Factors affecting Performance (18 points)*
   Given a user's program (written in a high level language like C), most computer architects will agree that the appropriate way to measure a processor's performance on that program is given by the following equation:

$$performance = \frac{machine\ instr.}{program} \times \frac{cycles}{machine\ instr.} \times \frac{time}{cycle}$$

   a. For each of the three terms, explain how ISA choices can affect that term.

   b. For each of the three terms, give a factor other than ISA which has an affect (ie three different factors).

2. *Reducing the Instruction Set (24 points)*
   Discuss the ways in which each of the instruction types given below might complicate a RISC style pipelined processor (a paragraph per part).

   a. Autoincrement addressing for loads/stores

   b. Absolute addressing for branch targets

   c. String Move

   Some issues you may wish to consider include

   - instruction encoding
   - interrupt handling
   - frequency that the instruction type might occur
   - ease with which the instruction type can be synthesized from simpler instructions
   - hazards introduced by pipelining that instruction with other instructions.

3. *RISC and CISC. What a lousy names. (12 points)*

Following Smith & Weiss, we compared the Alpha and PowerPC architectures. The article began with the following quote by P.Hester:

> At this point many RISC purists will undoubtedly claim that this is not a RISC design... This second generation RISC design, representing a reasonable melding of RISC and CISC concepts, is likely to be the direction of many future RISC designs.

Despite this "melding", I would claim that the PowerPC is far more similar to the Alpha (a very RISC processor) than it is to the VAX (the canonical CISC processor).

State the major differences between RISC and CISC architectures. Then support or refute my statement (NOT P.Hester's) by explaining where the PowerPC lies with respect to these differences.

4. *Faster Processors (25 points)*

What problems that occur in modern superscalar and/or superpipelined processors do each of the following techniques/units solve? Explain briefly (1-3 sentences) how the unit/technique solves the problem.

a. ROB

b. multiple integer ALUs

c. Tomasulo's algorithm and its derivatives

d. separate ALU and MEM pipeline stages

e. explicitly set instead of implicitly set condition codes

5. *Instruction Level Parallelism (15 points)*

a. Define a "sequential execution architecture".

b. How do the dataflow and VLIW architectures differ from the sequential execution architecture?

c. Give one example of how the MIPS R2000 ISA fails to support the sequential execution architecture assumption, and why this failure is a problem.

6. *All these funky units... (18 points)*

The figure on the following page is a functional unit diagram of the Alpha 21264 microprocessor (from “Digital 21264 Sets New Standard”, Linley Gwennap, *Microprocessor Report*, October 28, 1996, p.11 and provided in the last article package). In studying advanced processors, we have divided the pipeline into 5 major stages:

1. Fetch
2. Dispatch
3. Issue
4. Execute
5. Commit

In your exam booklet, make a table with three columns. On the left will be the letters corresponding to the functional units listed below. Beside each letter (in the middle column) will be the number(s) of the stage(s) in which that unit is used. On the right will be short explanations of why that unit is used in those stage(s) (1 sentence per stage in which the unit is used).

For example, if the branch predictor unit was given letter “z”, your exam booklet should have the following line:

unit	stage(s)	why?
z	1	to determine which instructions to fetch despite conditional branches

a. Instruction Cache & TLB

b. Retire Unit / Decode & Rename Regs

c. Integer / FP Instruction Queues

d. Addr ALU / Int Unit / FP Add.../ FP Mul

e. Int. Regs / FP Regs

f. Data Cache & TLB

g. L2 Cache & Bus Interface

For this figure, see the article (handed out in class) listed above