General Processor Information

(Last Modified: November 7, 1995)

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		Vdd (V)	Tech (um)	Met	Power (W)		Size (mm^2)	Xsistor (10^6)
						int	fp	int	fp			kB	Assoc				peak	typ		
Intel x86	i386SX	[41]	88	v/32	33	6.2	3.3			1/1	4/na/na	NA	NA	5.0	1.0	2	~2		43	0.28
	i486	[45]	89	v/32	33					2/1	5/na/5?	8 u.	4	5.0	1.0	2				1.2
	i486DX	[10]	91	v/32	50	27.9	13.1			2/1	5/na/5?	8 u.	4	5.0	0.8	3	5.0	3.9	81	1.2
	i486DX2	[20]	91	v/32	66	32.2	16.0			2/1	5/na/5?	8 u.	4	5.0	0.8	3	7.0	4.9	81	1.2
	i486DX4	[42]	93	v/32	99	51	27			2/1	5/na/5?	16 u.	4?	3.3	0.6	4		4		1.6
	P5	[2,10]	93	v/32	66	78	63.6			3/2	5/na/8	8/8	2/2	5.0	0.8	3	16.0		296	3.1
	P54VRT	[vi]	94	v/32	75	89.1	68.5			3/2	5/na/8			2.9	0.6	4	5.2	2.4		
		[vi]	94	v/32	90	110	84.4			3/2	5/na/8			2.9	0.6	4	6.5	3.0		
	P54C	[2,11]	94	v/32	100	122	93.2			3/2	5/na/8	8/8	2/2	3.3	0.6	4	5.0		163	3.1
	P54CQS	[47,vi]	95	v/32	120	172	108	3.7	2.8	3/2	5/na/8	8/8	2/2	3.3	0.35	4	10.0		163	3.1
	P54CS	[53,vi]	95	v/32	133	191	121	4.1	3.1	3/2	5/na/8	8/8	2/2	2.9	0.35	4				
	P55C	[31]	95	v/32	155					3/2	5/na/8				0.35	4				
	P6	[vi]	95	v/32	150	276	220	6.1	5.4	7/3[4]	14/14/16[4]	8/8[A]		3.1	0.6	4	29.2	23.2	306	5.5
		[vi]	95	v/32	200	366	283	8.1	6.7	7/3[4]	14/14/16[4]	8/8[A]		3.3	0.35	4	35	28.1	195[A]	5.5
		[vi]	96	v/32	166	327	261	7.1	6.2	7/3[4]	14/14/16[4]	8/8[B]		3.3	0.35	4	29.4	23.4	195[A]	5.5
Cyrix x86	5x86 (M1sc)	[vi]	95	v/32	100					2/1	6/6/?	16 u.	4	3.45	0.65	3	3.5	3	144	2.0
		[vi]	95	v/32	120					2/1	6/6/?	16 u.	4							2.0
	6x86 (M1)	[46]	95	v/32	100					3/2	7/7/?	16 u.	4	3.3	0.65	3	10		394	3.0
		[pn,vi]	95	v/32	120					3/2	7/7/?	16 u.	4	3.3	0.65	5			225	3.0
		[pn,vi]	96	v/32	>133					3/2	7/7/?	16 u.	4	3.3	0.5	5			169	3.0
Nexgen	Nx586	[42,43]	95	v/32	93					5/1[4]	7-9[4]	16/16		4.0	0.5	5	16	9	199	3.5
	Nx686	[vi]	95	v/32	180					7/4		16/32	2/2		0.35	5				~6
AMD	Am486	[pn]	95	v/32	120					2/1					0.5	3		~3		
	Am5x86	[vi]	95	v/32	133					2/1		16 u.			0.35	3				
	K5	[39,vi]	95	v/32	100	130				6/3	5/5/5?	16/8	4/4	3.3	0.35	3			161	4.3

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		Vdd (V)	Tech (um)	Met	Power (W)		Size (mm^2)	Xsistor (10^6)
						int	fp	int	fp			kB	Assoc				peak	typ		
Mot 68k	68020	[45]	85	v/32	25	NA	NA			1/1	?/na/na	NA/.25	NA/1	5.0	1.5	2				
	68030	[41,45]		v/32	50		NA			1/1	3/na/na	.25/.25	1/1	5.0	1.2	2			55	0.27
	68040	[10,45]	89	v/32	25	21	15			2/1	6/na/6	4/4	4/4	5.0	0.8	3	6.0		164	1.2
	68060	[15,21]	93	v/32	50	~60[2]	~45[2]			3/2	8/na/8	8/8	4/4	3.3	0.5	3	3.9		198	2.4
Power PC	601	[15,25]	93	32	50	40	60			4/3	4/5/6	32 u.	8	3.6	0.6	4	9.1	6.5	121	2.8
	601+	[9]	94	32	100	105	125			4/3	4/5/6	32 u.	8	3.3	0.5	5	5.6	4.0	74	2.8
	602	[43]	95	32	66	40				4/2	4?/5?/6?	4/4	2/2	3.3	0.5	4		1.2	50	1.0
	603	[2,6,25]	94	32	80	75	85			4/2	4/5/6	8/8	2/2	3.3	0.5	4	3.0	2.2	85	1.6
	603e	[44]	95	32	100	120	105			4/2	4/5/6	16/16	4/4	3.3	0.5	4	3.5		98	2.6
	603ev	[mw]	96	32	166	165	150			4/2	4/5/6	16/16	4/4	2.5	0.35	5		2.5	81	2.6
	604	[7,8]	94	32	100	128[8]	120[8]			6/4-	4/5/6	16/16	4/4	3.3	0.5	4	13.0	9.0	196	3.6
		[53]	95	32	133	176[8]	157[8]	4.1	3.3	6/4-	4/5/6	16/16	4/4	3.3	0.5	4		14	196	3.6
	604e	[mw]	96	32	150	250									0.35					
	613	[mw]	97		166	230														
	614	[mw]	97		266	500														
	615[9]	[mw]	96	32	150	220(i) PPC														
						138(i) x86														
	620	[pn,43]	95	64	133	225	300			6/4-	4/5/6	32/32	8/8	3.3	0.5	4	30.0		311	6.9
	630	[mw]	97?	64?	600	600														
Alpha	21064	[1,4,23]	92	64	200	133	200			4/2-	7/7/10	8/8	1/1	3.3	0.75		30.0		234	1.68
	21064a	[18,23]	94	64	275	194	293	4.2	6.3	4/2-	7/7/10	16/16	1/1	3.3	0.5	4	33.0		164	2.8
		[vi]	95	64	300	220	300			4/2-	7/7/10	16/16	1/1	3.3	0.5	4				2.8
	21066a	[34,37]	94	64	233	94	110			4?/2-	7/7/10	8/8	1/1	3.3	0.5	4	23.0		161	1.75
	21164	[22,21]	94	64	300	341	513	7.3	12.2	4/4-	7/7/9	8/8[I]	1/1	3.3	0.5	4	50.0		299	9.3
		[vi]	95	64	333	400	570			4/4-	7/7/9	8/8[I]	1/1	3.3	0.5	4				9.3
	21164a	[vi]	96	64	>417	~500				4/4-	7/7/9	8/8[I]	1/1	3.3	0.35					9.3

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						int	fp	int	fp			kB	Assoc				peak	typ		
Sparc	CY7C601	[19,20]	90?	32	40	21.8	22.8			1/1	5/na/na	na/na	na/na	5	0.8	2	3			
	Micro	[20,41]	91?	32	50	26.4	21.0			1/1		4/2		5	0.8	2	4		225	
	Weitek 2x	[20]	92?	32	80	32.2	31.1			1/1		16/8			0.8					1.8
	Micro 2	[20,37]	94	32	85	64.0	54.6			1/1	5/na/5?	16/8			0.5	3			233	2.3
		[vi]	95	32	110	76	65			1/1	5/na/5?	16/8			0.4					2.3
	Hyper (Ross)	[20]	93?	32	72	80	105			4/2-	6/6/6	8/na	?/na							
		[37]	94	32	100	103	127			4/2-	6/6/6	8/na	?/na		0.5	3			327[3]	1.7[3]
		[49]	95	32	125	159	183			4/2-	6/6/6	8/na	?/na		0.4					
		[pn]	95	32	150	180	245			4/2-	6/6/6	8/na	?/na							
		[pn]	96	32	200	235				4/2-	6/6/6	16/na			0.35					
	Super	[10,20]	92	32	60	89	103			5/3	4/4/5	20/16	5/4	5.3	0.6	3	14.2		256	3.1
	Super 2	[29,37]	95	32	90	135	147			5/3	4/4/5	20/16	5/4	5?	0.6	3	16		299	3.1
	Thunder 1	[21]	93	32	50	120	240			8/4				5	0.6					~6
	Ultra	[35,43]	95	64	167	275	305			9/4	9/9/9	16/16	2/1	3.3	0.5	4	~30		315	5.2
	Ultra II	[vi]	96	64	250	~350	~550							2.5	0.35	5				5.4
	Ultra III	[vi]	96/7	64		1000	1500													
	R1 (HaL)	[43]	95	64	154	256	330			9/4	4/6/7	64/64[6]	4/4	3.3	0.4	4	?/60[7]			2.7/ 21.9[7]
ARM	610	[3,15,27]	93	32	25	16	NA			1/1	3/na/na	4 u.	64	5.0	1.0	2	0.5		71	0.36
	710	[27]	94	32	33		NA			1/1	3/na/na	8 u.	4	5.0	0.8	2	0.5		46	0.54
	SA-1	[vi]	96	32	160					1/1	5/5?/5?			2.0	0.35	3	0.5			
Hobbit	92010	[3,15]	92	32	20	8	NA			1/1	3/na/na			3.3	0.9		0.25			
	92020S	[40]	94	32																

Processor		Source	Date (ship)	Bits (i/d)	Clock (MHz)	SPEC-92		SPEC-95		Units / Issue	Pipe Stages int/ldst/fp	Cache (i/d)		V_{dd} (V)	Tech (um)	Met	Power (W)		Size (mm^2)	Xsistor (10^6)
						int	fp	int	fp			kB	Assoc				peak	typ		
MIPS	R3000	[12,20]	88?	32	40	27.9	35.8			1/1	5/na/na	na/na	na/na	5.0	1.2		4.0			
	R6000[5]	[20,32]	91	32	66.7	40.6	45.1			1/1	5?/na/na	na/na	na/na						[5]	
	R4000	[20,32]	92	64	100	59	61			2/1	8/na/10	8/8	1/1		1.0				213	1.1
	R4200	[2,5]	93?	64	80	55	30			1/1	5/na/5	16/8	1/1	3.3	0.64	3	1.8	1.5	78	1.4
	R4300i	[52]	95	64	100	60	45			1/1	5/na/5	16/8	1?/1?	3.3	0.35			1.8	45	1.7
	R4400	[10,17]	92	64	150	88	97			2/1?	8/na/10	16/16	1/1	3.3	0.6	3	15		186	2.3
		[37,38]	94	64	200	141	143	3.9	?	2/1?	8/na/10	16/16	1/1	3.3	0.5	2			148	2.2
		[53]	95	64	250	180	178			2/1?	8/na/10	16/16	1/1	3.3	0.35				108	~2.2
	R4600	[13,37]	94	64	150	110	83			2/1	5/na/5	16/16	2/2	3.3	0.64	3	4.6	3.0	77	1.85
	R4700	[37]	95	64	175	~130	~100			2/1	5/na/5	16/16			0.6	3			73	1.85
	R8000	[20,37]	94	64	75	109	311			6/4-	5/5/?	16/16	1/1	3.3	0.7	3			596[3]	3.43[3]
		[vi]	95	64	90	132	396			6/4-	5/5/?	16/16	1/1							
	R10000	[28,29]	95	64	200	>300	>600			5/5	5/6/7	32/32	2/2	3.3	0.5	4	~30		298	5.9
PA-RISC	PA 1.1	[32]		32	66	51	82			1/1	5/na/na	na/na	na/na		1.0				196	0.58
	HARP-1	[41]		32	120	70	120													
	7100	[3, 10]	92	32	100	80	150	3.2	4.1	2/2-	5/na/6	na/na	na/na	5.0	0.8	3	23.0		202	0.85
	7150	[24]	94?	32	125	136	201	4.0	4.6	2/2-	5/na/6?	na/na	na/na	5.0	0.8	3	30		196	0.85
	7100LC	[24]	94	32	100	102	137	2.9	3.5	3/2	5/na/6?	1/na	?/na	5.0	0.8	3	~10		196	0.8
	7200	[24]	94	32	140	~150	~250	4.9	8.8	3/2	5/na/6?	na/2	na/64	4.4	0.55	3	30		210	1.26
	7300LC	[vi]	96	32	~150	~200	~275	~5.5	~7.3			64/64			0.5	3				9
	8000	[33,48]	95	64	200	>360	>550	8.6	15	10/4-	7/9/9	na/na	na/na		0.5	4			345	3.9
SH Hitachi	II	[21]	93	16/32	28.7	~8	NA			1/1	5/5/na	4 u.	4	5	0.8	3	0.4			
	III (7708)	[21]	94	16/32	60	~35	NA			1/1	5/5/na	8 u.	4	3.3	0.5	3	0.6		44	0.8

not available yet.

Power: peak power numbers used when available, else estimated from average power. Easier to find peak, rather than average.
Units: Functional units NOT including "system" units. **Issue**: Peak instructions issued per cycle; **"-"**: Indicates limitations on peak issue rate.

Cache: On-chip cache. **ETR**: Energy-Throughput Ratio = Watts/SPECvalue^2. Measure of Energy Efficiency. The lower, the better. For 1/ETR, the higher the better

1: The 21164 has an *on-chip* 96kB L2 cache.; The P6 has a 256kB L2 in the same MCM package as the (xistors not counted in total).

2: Estimated that x60 is 3 times the performance of the x40.

3: Combined total for 2 chips.

4: Data for the RISC-like core. (AMD: rops; NexGen: RISC86 instructions; Intel: uops)

5: This was an ECL implementation of the MIPS II ISA..

6: External (in an MCM package)

7: Single-chip CPU / Combined MCM package.

8: These are the highest SPEC numbers reported so far for the 604, which fall below the original estimates (100MHz - 160/165; 133MHz - 200/200)

9: This chip reportedly combines a Pentium and PPC604 on one chip (multiple die?).

A: The P6 has a 256kB L2 (15.5 million xsistors) in the same MCM package as the (xistors not counted in total).

B: The P6 has a 512kB L2 (31 million xsistors) in the same MCM package as the (xistors not counted in total).

SOURCES (* = Can be found in the CPU Info Center)

[1] = ISSCC92
[2] = ISSCC94
[3] = Hot Chips IV
[4]* = http://netlib2.cs.utk.edu/performance/html/PDStop.html
[5]* = Preliminary Product Sheet for R4200
[6] = to be published.
[7]* = Press Release 4/19/94: 100MHz PPC604
[8] = uP 4/94 (as reported by M. Horowitz)
[9]* = Press Release 3/30/94: 100MHz PPC601
[10] = Spectrum 12/93
[11] = to be published.
[12] = Courtesy M. Horowitz, SPEC Table
[13]* = Product Sheet for R4600
[15] = CompCon 93
[16] = CompCon 94
[17]* = Product sheet for R4400
[18]* = DEC Press Release.
[19] = CY7C601 Data Book
[20] = SPECtable from John Dimarco.
[21] = Hot Chips 94.
[22]* = DEC Press Release 9/7/94
[23]* = John DiMarco's SPEC Table.
[24]* = HP's Online server (http://www.wsg.hp.com/wsg/Strategy/strategy.html)
[25]* = PowerPC White Papers (http://www.austin.ibm.com/tech/p2ppc_tech.html)
[27] = from Dave Jaggar, chief architect of the ARM.
[28]* = MIPS Press release
[29] = 10/17/94 EE Times
[30] = 10/10/94 EE Times
[31]* = Computergram News
[32] = A Guide to RISC Microprocessors, Michael Slater, 1992.
[33]* = from comp.arch (http://infopad/~hbd/gpp/announce/pa8000_overview)
[34] = 11/21/94 EE Times
[35] = Leslis Kohn, "Ultrasparc", Invited Speaker, Micro 27 Conf.
[36] = from comp.arch -- Alain Lachapelle (alainl@cam.org)
[37] = uP 12/26/94
[38]* = MIPS Home Page (http://www.mips.com)
[39] = uP 10/24/94
[40] = uP 1/24/94
[41]* = CHIPS and SYSTEMS SPEC Chart, by Gary Snow
(http://infopad.eecs.berkeley.edu/~hbd/gpp/summary/snow_survey)
[42]* = CHIPLIST 7.2 by Aad Offerman
(http://einstein.et.tudelft.nl/~offerman/chiplist.html)
[43] = ISSCC95
[44] = Motorola PPC Homepage:
(http://www.mot.com/PowerPC/prodinfo.html)
[45] = Advanced Microprocessors, Daniel Tabak, 1991
[46] = uP 2/16/94
[47]* = Intel Press Release
[48] = Compcon 95.
[49] = Electronic News 3/20/95
[52]* = Press Release 4/17/95
[53] = uP 6/19/95

[vi] = Vendor Info
[vp]* = Vendor Press Release
[pn]* = PowerPC News
[mw] = MacWeek (online)

NOTE: Hobbit SPEC calculated from 28k Drystones ~= 8 SPECint92
Hobbit = 27k Dry @ 20 MHz