| CPSC 418 | Advanced Computer Architecture | Spring 1995 |
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# Midterm: 9 Feb

## General Information

- 100 points total
- Closed book, closed notes
- Time limit: 1 hour, 15 minutes
- **Show all relevant work**:
  - Write neatly
  - Write all formulas out with variables, then substitute in numerical values and evaluate the formula
  - Document the meaning of all variables you use

**Problem 1** (8 Points)

To keep up with the market (*e.g.* other companies), system performance needs to double every year. You are considering a design improvement that will increase performance by 10% but delay the release date of a system by two months.

In terms of the performance of the system with respect to other machines that will be on the market when it will be released, is it better to release the system on its current schedule, or add the improvement and move back the release by two months?

**Problem 2** (10 Points)

This problem refers to the pipeline shown in Figure 2, where the stages perform their normal functions. In particular:

- Branch prediction is performed in the Decode stage.
- Branch instructions test a general purpose register.

**2(a)** (5 Points) What is the penalty (in number of cycles) for a branch mispredict?

**2(b)** (5 Points) Must all microprocessors in this architectural family have the same penalty for branch mispredictions? Justify your answer.

**Problem 3** (10 Points)

Two microprocessors (R, for "rabbit" and T for "turtle") from different architectural families have the same memory hierarchy (levels of cache, sizes, speed of memory, *etc.*).

The clock speed for Micro-R is 1.5 times faster than the clock in Micro-T.

For the SPEC benchmarks on Micro-T:

| | |
|---|---|
| 3 cycles | average memory latency |
| 2.4 cycles | average CPI for load instruction (including memory access time) |

**3(a)** (5 Points)

Do you have enough information to calculate the average memory latency in clock cycles for the SPEC benchmarks running on Microprocessor R? If so, do so. If not, explain what additional information you need.

**3(b)** (5 Points)

Do you have enough information to calculate the average CPI for a load instruction (using the SPEC benchmarks) for Microprocessor R? If so, do so. If not, explain what additional information you need.

**Problem 4** (12 Points)

In the table below list:

1. three different architectures
2. two different microprocessors for each architecture

| | 1 | 2 | 3 |
|---|---|---|---|
| Architecture | | | |
| Microprocessor 1 | | | |
| Microprocessor 2 | | | |

For each architecture, list one distinguishing feature of the architecture or of a microprocessor in the architecture.

- Distinguishing feature for architecture 1

- Distinguishing feature for architecture 2

- Distinguishing feature for architecture 3

**Problem 5** (35 Points)

You have a workstation that is used almost exclusively for floating-point intensive programs, such as Spice.

Currently, it does not have a cache, and you are using a simple, non-optimizing compiler.

You can afford to spend up to \$700 on upgrading the computer. You can either buy SRAM for a cache or an optimizing compiler, which sells for \$500.

**5(a)** (25 Points)

Using the tables and figures at the end of the test, find the relative speedup for using the optimizing compiler and upgrading the cache with the maximum amount of SRAM you can buy for \$700.

**5(b)** (10 Points)

In terms of the price/performance ratio, is it better to buy the cache or the compiler?

**Problem 6** (25 Points)

For the pipeline in Figure 2:

- divides spend a total of two cycles in the divide stage.
- load/stores use the load/store stage once
- stores do not use the writeback stage

Using the standard style used in class, complete the execution table in Figure 1 for the following program:

```
; R1=A, R2=B, R3=C, R4=D, R5=E
1000   ADD R1, R3, R1
1004   DIV R3, R2, R1
1008   ADD R3, R1, R5
100C   LDW R2, R5
```

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PC | | | | | | | | | | | | | | |
| FI | | | | | | | | | | | | | | |
| DI | | | | | | | | | | | | | | |
| FO | | | | | | | | | | | | | | |
| EX | | | | | | | | | | | | | | |
| LS | | | | | | | | | | | | | | |
| DIV | | | | | | | | | | | | | | |
| WB | | | | | | | | | | | | | | |
| BY1 | | | | | | | | | | | | | | |
| BY2 | | | | | | | | | | | | | | |
| S1 | | | | | | | | | | | | | | |
| S2 | | | | | | | | | | | | | | |
| R1 | | | | | | | | | | | | | | |
| R2 | | | | | | | | | | | | | | |
| R3 | | | | | | | | | | | | | | |

Figure 1: Execution table

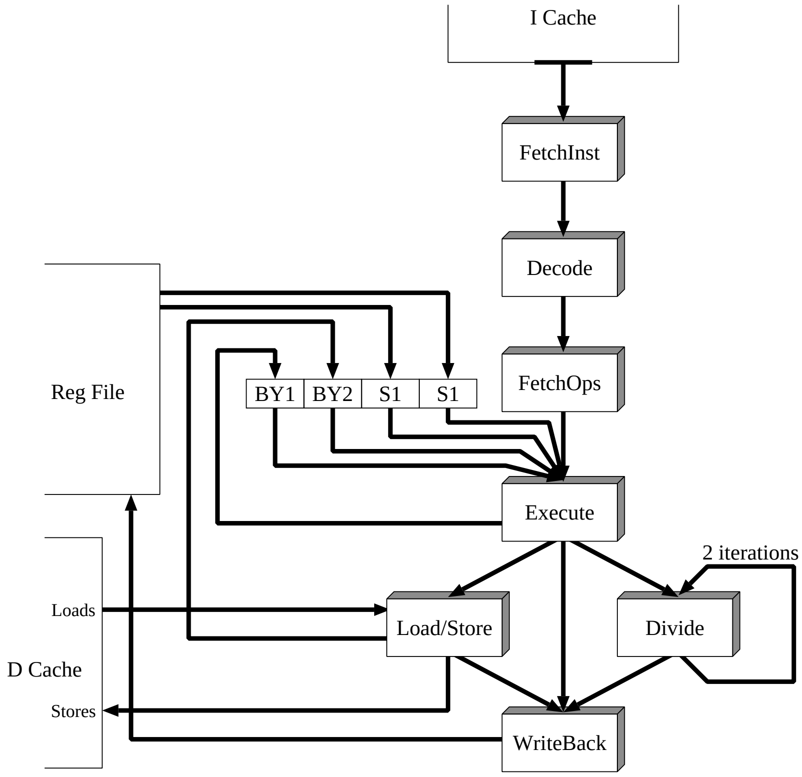


Figure 2: Pipeline for sample microprocessor

| | |
|---|---|
| \$400 | 512k |
| \$600 | 1024k |
| \$1000 | 2048k |

Figure 3: SRAM prices

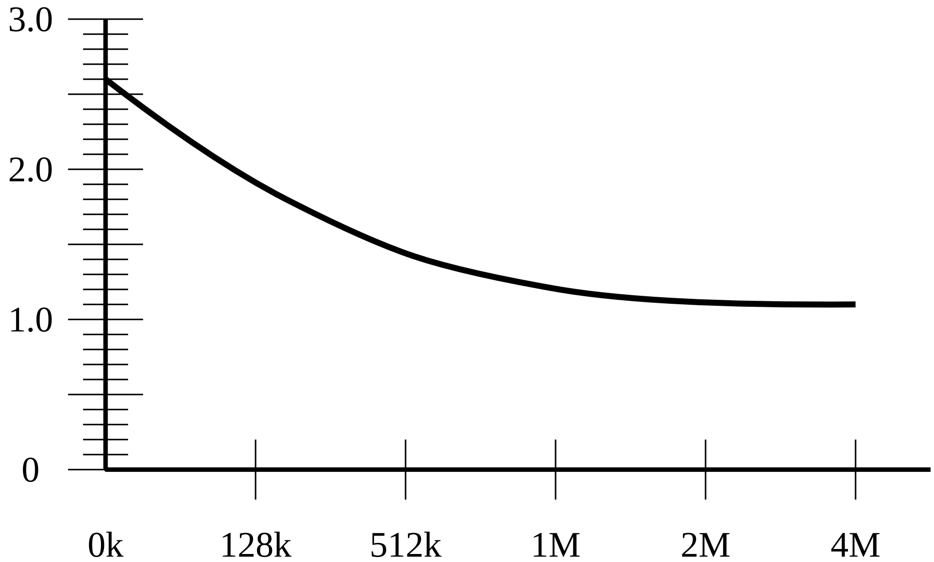


Figure 4: CPI versus cache sizes for sample microprocessor

Figure 5: Absolute instruction counts for optimized and unoptimized code for sample microprocessor

Figure 6: Effects of optimization on instruction mix for sample microprocessor

Figure 7: Effect of number of registers on number of memory references for Spice on sample microprocessor