CPSC 418 **Advanced Computer Architecture** **Spring 1995**

Homework 10 (NO CREDIT): Due 30 Mar

Note

- This homework is for your use in studying for the final (Tue 4 April, in Angus 223).
- The assignment is not worth any points, and will not be graded.
- We will discuss the assignment in class on Thur 30 Mar, and the solutions will be handed out then.

Problem 1 (0 Points)

1. Pipelines
   (a) definition
   (b) how does pipelining improve the performance of a microprocessor
   (c) give upper and lower bounds on the number of stages in typical microprocessors' pipeline
   (d) why not have fewer or more stages in a pipeline?
2. Superscalar
   (a) definition
   (b) how does "superscalar-ing" improve the performance of a microprocessor
   (c) give upper and lower bounds on the "superscalar-edness' in typical microprocessors
   (d) why not have more or less "superscalar-edness" in a microprocessor?
3. Caches
   (a) definition
   (b) how do caches improve the performance of a microprocessor
   (c) give upper and lower bounds on the number and sizes of caches in typical microprocessors
   (d) what design decisions must be made in designing a cache system
   (e) why not have more or bigger caches in a microprocessor?
4. Register renaming
   (a) definition

   (b) how does register renaming improve the performance of a microprocessor
   (c) what design decisions must be made in designing a register renaming system

5. Multiple / Duplicate functional units
   (a) give an example of a typical configuration for a microprocessor with multiple and/or duplicate functional units
   (b) how do multiple and/or duplicate functional units improve the performance of a microprocessor
   (c) what design decisions must be made in designing a microprocessor with duplicate and/or multiple functional units

Problem 2 (0 Points) You are considering three options for a new microprocessor design. Assuming that average performance doubles each year, decide which option results in the best price/performance ratio for the microprocessor at the time it will be introduced on the market. Assume that all of the options add the same cost to the product.

Design decisions already made:

Generic RISC instruction set (*e.g.* DLX).

Single issue. (With current design, CPI is predicted to be = 1.3, *ignoring all stalls caused by memory accesses and control hazards.*)

An on-chip 4k instruction cache: 2-way set associative with 32 byte blocks. Access time for a hit is 1 cycle. On a cache miss, the entire block must be read in from main memory before the instruction is available.

There is one dual-word read/write port on the main memory and one dual-word read port. The read/write port is connected to the load/store unit of the CPU and the read port is connected to the instruction cache. The latency for accessing a single or double word in main memory is 100 ns. A 32 byte block can be transferred to or from main memory in 180 ns.

Clock speed = 10ns / cycle.

Statically predict branches as not taken. Branch targets are calculated in the Decode (second) stage. Branch taken/not-taken determined in the Fetch Operands (third) stage.

Options:

small on chip caches Upgrade the 4k instruction cache to 8k and add an 8k data cache. Both caches are 2-way set associative and have 32 byte blocks. The data cache is write-through and at any time 50% of the blocks are dirty. Access latency = 1 cycle for hits.

branch prediction Add a branch-target buffer (BTB) for conditional branches only. Buffer hit rate = 85%; when a miss occurs the branch is predicted as not-taken and execution proceeds as without the BTB. Prediction correctness for branches that hit in BTB = 90%. The additional control circuitry required for the branch-target buffer will cause the clock cycle to increase to 12ns. Additional development time = 3 months.

register-renaming Adding register renaming can cut the average CPI (not including memory or control stalls) from 1.3 to 1.15. Additional development time = 6 months.

Problem 3 (0 Points) What are the key differences between scoreboards, reservations stations, and register renaming?

Problem 4 (0 Points) There are many other topics to study that don't appear on this homework, this includes (but is not limited to):

1. Pipeline execution diagrams
2. "Simulations" of Scoreboards, Reservation stations, Register-renaming
3. Data hazards
4. Calculating number and types of memory references, instruction distributions
5. Any other topic that appeared on a homework assignment