CPSC 418	Advanced Computer Architecture	Spring 1995

Final: 4 April

General Information

- 100 points total
- Closed book, closed notes
- Time limit: 2 hour, 30 minutes
- **Show all relevant work**:
  - Write neatly.
  - Write all formulas out with variables, then substitute in numerical values and evaluate the formula.
  - Document the meaning of all variables you use.
  - Justify all of your answers.

Name:

Student Id Number:

Problem 1 (12 Points)

A company is working on a tight deadline to produce a new microprocessor. If they upgrade to a more powerful set of CAD tools, they can move the completion date of their design $1\frac{1}{2}$ months earlier, but the cost of the tools will increase their price per chip by 10%. Assuming that the average price/performance ratio improves by a factor of 2 every year, should they buy the new tools?

Problem 2 (16 Points)

This question uses the fragment of assembly language in Figure 1.

```
100   DIV  R5, R7, R2
101   ADD  R4, R3, R5
102   SUB  R6, R2, R4
103   MUL  R4, R1, R2
104   ADD  R7, R3, R2
105   MUL  R5, R7, R6
```

Figure 1: Code for data hazard analysis

2(a) (6 Points)

Find and classify all of the data hazards (write your answer in Table 1). For each hazard, identify the line numbers of the two instructions that are involved in the hazard, the type of hazard, and the data location.

Table 1: Find and classify data hazards

Instruction 1	Instruction 2	Hazard Type	Data Location/Value

2(b) (10 Points)

For this question, use the table on the following page to write your answer.

Given a microprocessor with:

- 1 Add/Sub unit, latency = 2 cycles, throughput = 1 inst/cycle
- 1 Multiply unit, latency = 5 cycles, throughput = 1 inst/cycle
- 1 Divide unit, latency = 20 cycles, non-pipelined

For each instruction in Figure 1, say whether the instruction would stall in a microprocessor using register renaming. If the instruction would stall, say why it stalls and what stage it stalls in (*e.g.* Issue/RegRename, Queue, Execute, or WriteBack).

Note:

- Initially all functional units are available and all registers have valid data.
- There are two reservation stations or queue slots per functional unit.
- There are enough physical registers that the freelist always has registers on it.

`100 DIV`	Stall/NoStall	Location	Cause
`101 ADD`			
`102 SUB`			
`103 MUL`			
`104 ADD`			
`105 MUL`			

Problem 3 (12 Points) List two aspects of computer architecture and/or implementation that have changed significantly over time.

How did these changes affect the price and/or performance of computers?

Give two examples (implementation or design choices, names of machines, *etc.*) that illustrate these changes.

Problem 4 (12 Points)

For an "average" general-purpose microprocessor running "average" programs, which of the following will give the largest performance increase — *justify your answer.*

1. increase clock speed of CPU by 10%
2. decrease average memory access time for instruction fetch by 10%
3. decrease latency of integer multiply by 5%
4. decrease average memory access time for data by 40%

Problem 5 (22 Points)

This problem examines memory access times, CPI, and performance for the Intel 8086 and the DLX.

Table 2: Memory System

Main memory access time	10 cycles
Block transfer between cache and main memory	20 cycles
L1 Icache	32k 4-way set assoc 1 cycle access time
L1 Dcache	32k direct-mapped 1 cycle access time write-allocate, write-back %dirty blocks = 50%

Table 3: Microprocessors

Microprocessor	CPI w/o stalls caused by memory accesses
Intel 8086	10.0
DLX	1.3

5(a) (5 Points)

For each of the two microprocessors, find the:

- average memory access time for instruction fetch
- average memory access time for data

5(b) (5 Points)

Find the real CPI for an Intel 8086 and a DLX using the memory system described in part (a).

5(c) (4 Points)

Of the two microprocessors (Intel 8086 and DLX) which one's performance is more affected by the performance of the memory system? *justify your answer*

5(d) (4 Points)

The Intel 8086 is a non-pipelined microprocessor. Newer microprocessors in the x86 family are pipelined, and the Pentium and P6 (80686) are superscalar.

How do you think the CPI value of the 8086 compares to that of the more recent x86 microprocessors? (*e.g.* Much lower than the P6, a little higher, about the same, etc). *justify your answer*

5(e) (4 Points)

Based upon this example, do you think memory system design is more important for the 8086 or the Pentium? *justify your answer*

Problem 6 (22 Points)

This problem examines some of the performance tradeoffs of the BCT instruction in the IBM Power architecture.

The IBM Power architecture includes a BCT conditional branch instruction that decrements a special register and then jumps to the specified address if the resulting value is greater than or equal to zero.

This instruction is used to simplify inner loops in programs. It replaces an addition, followed by a compare (The `S_` instructions in the DLX), followed by a conditional branch

Note: it could also replace a subtract instruction followed by a conditional branch, but subtracts account for less than 1.5% of instructions, so we will ignore them in this problem.

Given the information and assumptions below, what would the performance tradeoff be if a BCT instruction was added to the DLX?

- Branches in the DLX use PC relative addressing mode and test general purpose registers.
- We are using the DLX pipeline, which differs from the pipeline in lecture in that the Decode and FetchOperands stages are combined together: (FetchInst, Decode/FetchOps, Execute, WriteBack)
- Statically predict all conditional branches as not taken.
- 50% of the backwards conditional branches are for inner loops that could use BCT.
- With the BCT instruction, decrementing the index register and comparing the result to zero is done in the second stage.
- Adding the BCT would increase the clock cycle by 5%.
- The actual CPI (*i.e.* including stalls) of the standard DLX is 1.6